

# NC7SZ57, NC7SZ58

## TinyLogic® UHS Universal Configurable 2-Input Logic Gates

### Features

- Space saving SC70-6 lead surface mount package
- Ultra small MicroPak™ leadless package
- Ultra High Speed
- Capable of implementing any 2-input logic function
- Typical usage replaces 2 TinyLogic® gate devices
- Reduces part counts in inventory
- Broad  $V_{CC}$  operating range: 1.65V to 5.5V
- Power down high impedance input/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

### General Description


The NC7SZ57 and the NC7SZ58 are Universal Configurable 2-Input Logic Gates. Each device is capable of being configured for 1 of 5 unique 2-input logic functions. Any possible 2-input combinatorial logic function can be implemented as shown in the Function Selection Table. Device functionality is selected by how the device is wired at the board level. Figure 1 through Figure 10 illustrate how to connect the NC7SZ57 and NC7SZ58 respectively for the desired logic function. All inputs have been implemented with hysteresis.

The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad  $V_{CC}$  operating range. The device is specified to operate over the 1.65V to 5.5V  $V_{CC}$  operating range. The input and output are high impedance when  $V_{CC}$  is 0V. Inputs tolerate voltages up to 5.5V independent of  $V_{CC}$  operating range.

### Ordering Information

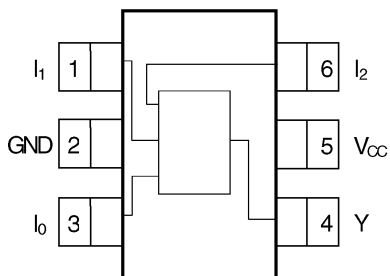
Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ57P6X	MAA06A	Z57	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ57L6X	MAC06A	KK	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel
NC7SZ58P6X	MAA06A	Z58	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ58L6X	MAC06A	LL	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

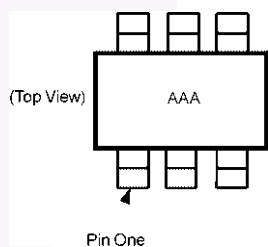
## Connection Diagrams

Pin Assignments for SC70



(Top View)  
NC7SZ57 and NC7SZ58

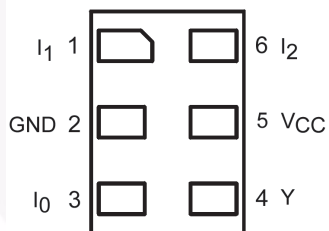
Pin One Orientation Diagram



AAA = Product Code Top Mark — see ordering code

**Note:** Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignment for MicroPak



(Top Thru View)

## Function Table

Inputs			NC7SZ57	NC7SZ58
			$Y = (\bar{I}_0) \cdot (\bar{I}_2) \cdot (I_1) \cdot (I_2)$	$Y = (I_0) \cdot (\bar{I}_2) + (\bar{I}_1) \cdot (I_2)$
I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>		
L	L	L	H	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	H
H	L	H	L	H
H	H	L	H	L
H	H	H	H	L

## Pin Description

Pin Name	Description
I <sub>0</sub> , I <sub>1</sub> , I <sub>2</sub>	Data Inputs
Y	Output

H = HIGH Logic Level

L = LOW Logic Level

## Function Selection Table

2-Input Logic Function	Device Selection	Connection Configuration
2-Input AND	NC7SZ57	Figure 1
2-Input AND with inverted input	NC7SZ58	Figure 7, Figure 8
2-Input AND with both inputs inverted	NC7SZ57	Figure 4
2-Input NAND	NC7SZ58	Figure 6
2-Input NAND with inverted input	NC7SZ57	Figure 2, Figure 3
2-Input NAND with both inputs inverted	NC7SZ58	Figure 9
2-Input OR	NC7SZ58	Figure 9
2-Input OR with inverted input	NC7SZ57	Figure 2, Figure 3
2-Input OR with both inputs inverted	NC7SZ58	Figure 6
2-Input NOR	NC7SZ57	Figure 4
2-Input NOR with inverted input	NC7SZ58	Figure 7, Figure 8
2-Input NOR with both inputs inverted	NC7SZ57	Figure 1
2-Input XOR	NC7SZ58	Figure 10
2-Input XNOR	NC7SZ57	Figure 5

## Logic Configurations NC7SZ57

Figure 1 through Figure 5 show the logical functions that can be implemented using the NC7SZ57. The diagrams show the DeMorgan's equivalent logic duals for a given 2-input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

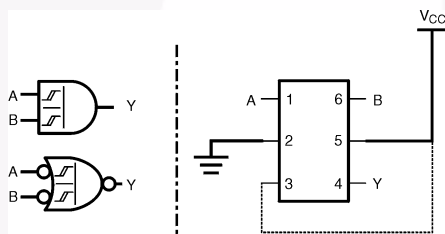


Figure 1. 2-Input AND Gate

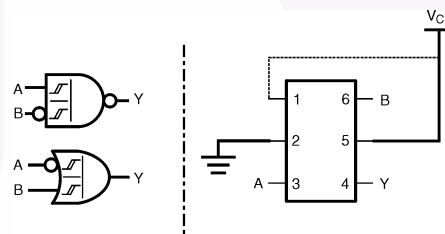


Figure 3. 2-Input NAND with Inverted B Input

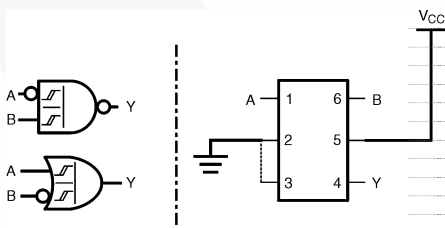


Figure 2. 2-Input NAND with Inverted A Input

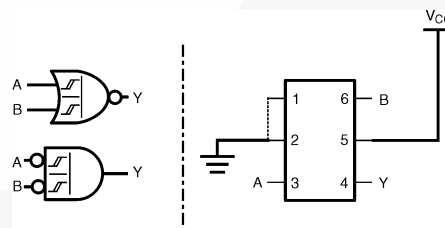


Figure 4. 2-Input NOR Gate

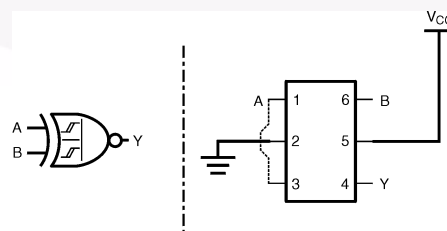


Figure 5. 2-Input XNOR Gate

## Logic Configurations NC7SZ58

Figure 6 through Figure 10 show the logical functions that can be implemented using the NC7SZ58. The diagrams show the DeMorgan's equivalent logic duals for a given 2-input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

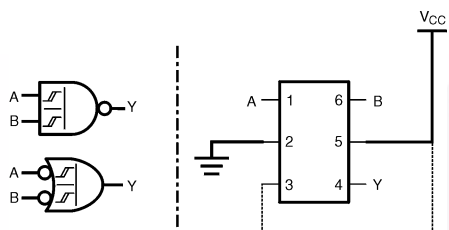


Figure 6. 2-Input NAND Gate

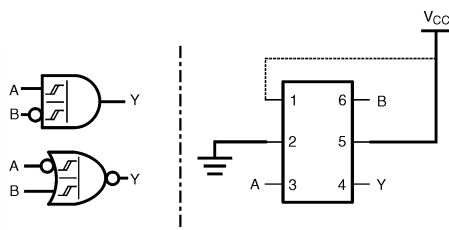


Figure 8. 2-Input AND with Inverted B Input

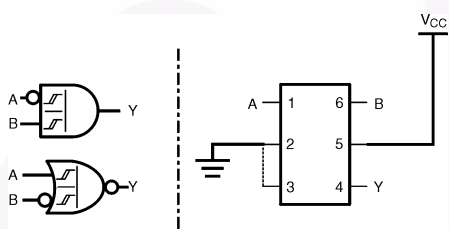


Figure 7. 2-Input AND with Inverted A Input

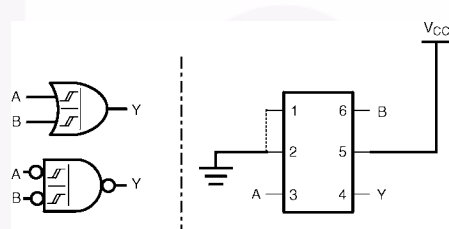


Figure 9. 2-Input OR Gate

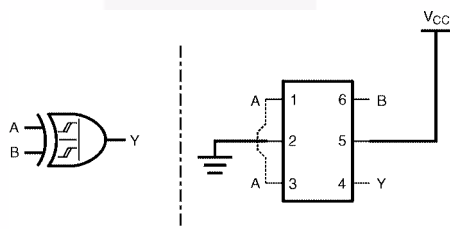


Figure 10. 2-Input XOR Gate

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7V
$V_{IN}$	DC Input Voltage	-0.5V to +7V
$V_{OUT}$	DC Output Voltage	-0.5V to +7V
$I_{IK}$	DC Input Diode Current @ $V_{IN} \leq 0.5V$	-50mA
$I_{OK}$	DC Output Diode Current @ $V_{IN} \leq -0.5V$	-50mA
$I_{OUT}$	DC Output Current Source/Sink Current	$\pm 50mA$
$I_{CC}/I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50mA$
$T_{STG}$	Storage Temperature Range	-65°C to +150°C
$T_J$	Max. Junction Temperature Under Bias	150°C
$T_L$	Lead Temperature (Soldering, 10 seconds)	260°C
$P_D$	Power Dissipation @ +85°C, SC70-6	180mW

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage Operating	1.65V to 5.5V
	Supply Voltage Data Retention	1.5V to 5.5V
$V_{IN}$	Input Voltage	0V to 5.5V
$V_{OUT}$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\theta_{JA}$	Thermal Resistance, SC70-6	350°C/W

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions		T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units				
					Min.	Typ.	Max.	Min.	Max.					
V <sub>P</sub>	Positive Threshold Voltage	1.65			0.6	0.99	1.4	0.6	1.4	V				
		2.3			1.0	1.39	1.8	1.0	1.8					
		3.0			1.3	1.77	2.2	1.3	2.2					
		4.5			1.9	2.49	3.1	1.9	3.1					
		5.5			2.2	2.95	3.6	2.2	3.6					
V <sub>N</sub>	Negative Threshold Voltage	1.65			0.2	0.50	0.9	0.2	0.9	V				
		2.3			0.4	0.75	1.15	0.4	1.15					
		3.0			0.6	0.99	1.5	0.6	1.5					
		4.5			1.0	1.43	2.0	1.0	2.0					
		5.5			1.2	1.70	2.3	1.2	2.3					
V <sub>H</sub>	Hysteresis Voltage	1.65			0.15	0.48	0.9	0.15	0.9	V				
		2.3			0.25	0.64	1.1	0.25	1.1					
		3.0			0.4	0.78	1.2	0.4	1.2					
		4.5			0.6	1.06	1.5	0.6	1.5					
		5.5			0.7	1.25	1.7	0.7	1.7					
V <sub>OH</sub>	HIGH Level Output Voltage	1.65	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100μA	1.55	1.65		1.55		V				
		2.3			2.2	2.3		2.2						
		3.0			2.9	3.0		2.9						
		4.5			4.4	4.5		4.4						
		1.65	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -4mA	1.29	1.52		1.29						
		2.3			I <sub>OH</sub> = -8mA	1.9	2.15		1.9					
		3.0				I <sub>OH</sub> = -16mA	2.4	2.80			2.4			
		3.0					I <sub>OH</sub> = -24mA	2.3	3.68			2.3		
		4.5						I <sub>OH</sub> = -32mA	3.8		4.20		3.8	
V <sub>OL</sub>	LOW Level Output Voltage	1.65	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100μA		0.0	0.10		0.10	V				
		2.3				0.0	0.10		0.10					
		3.0				0.0	0.10		0.10					
		4.5				0.0	0.10		0.10					
		1.65	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 4mA		0.08	0.24		0.24					
		2.3			I <sub>OL</sub> = 8mA		0.10	0.3			0.3			
		3.0				I <sub>OL</sub> = 16mA		0.15	0.4			0.4		
		3.0					I <sub>OL</sub> = 24mA		0.22		0.55		0.55	
		4.5						I <sub>OL</sub> = 32mA			0.22	0.55		0.55
I <sub>IN</sub>	Input Leakage Current	0–5.5	V <sub>IN</sub> = 5.5V, GND				±0.1			±1	μA			
I <sub>OFF</sub>	Power Off Leakage Current	0.0	V <sub>IN</sub> or V <sub>OUT</sub> = 5.5V				1		10	μA				
I <sub>CC</sub>	Quiescent Supply Current	1.65–5.5	V <sub>IN</sub> = 5.5V, GND				1		10	μA				

## AC Electrical Characteristics

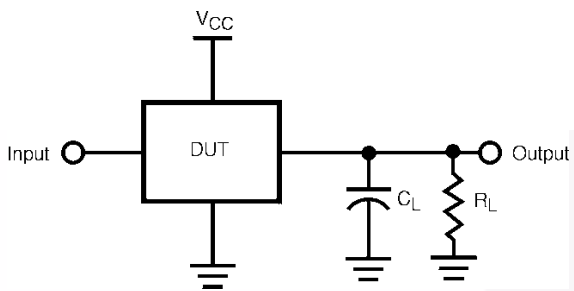
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Fig. No.
				Min.	Typ.	Max.	Min.	Max.		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Y	1.8 ± 0.15	C <sub>L</sub> = 15pF, R <sub>L</sub> = 1MΩ	3.0	8	14.0	3.0	14.5	ns	Figure 11 Figure 13
		2.5 ± 0.2		1.5	4.9	8.0	1.5	8.5		
		3.3 ± 0.3		1.2	3.7	5.3	1.2	5.7		
		5.0 ± 0.5		0.8	2.8	4.3	0.8	4.6		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Y	3.3 ± 0.3	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	1.5	4.2	6.0	1.5	6.5	ns	Figure 11 Figure 13
		5.0 ± 0.5		1.0	3.4	4.9	1.0	5.3		
C <sub>IN</sub>	Input Capacitance	0			2				pF	
C <sub>PD</sub>	Power Dissipation	3.3	(1)		14				pF	Figure 12
	Capacitance	5.0			17					

**Note:**

- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 12) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:

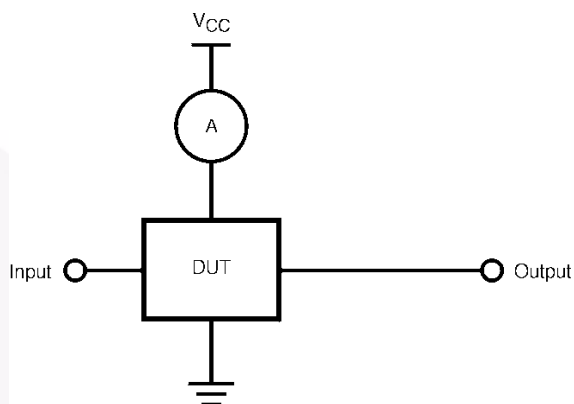
$$I_{CCD} = (C_{PD})(V_{CC})(f_{in}) + (I_{CCStatic}).$$

### AC Loading and Waveforms



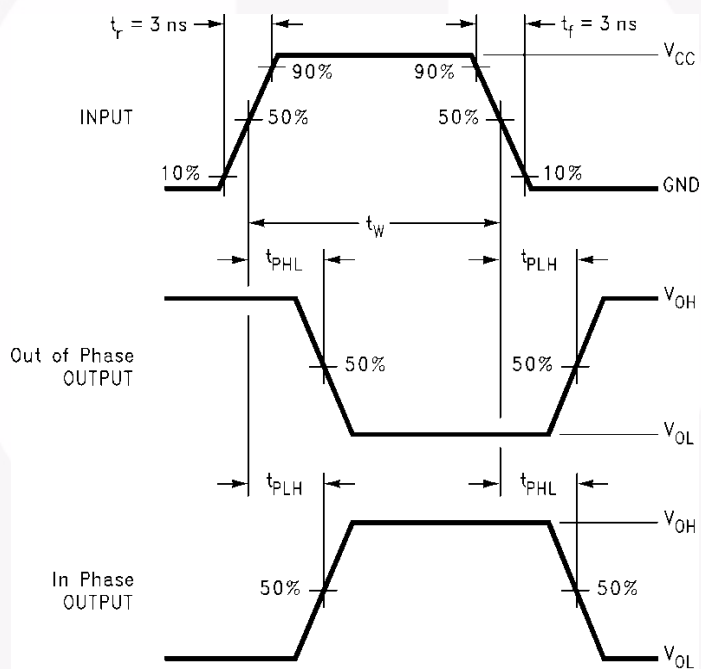
$C_L$  includes load and stray Capacitance  
 Input PRR = 1.0 MHz,  $t_W = 500$  ns

**Figure 11. AC Test Circuit**



Input = AC Waveforms  
 PRR = Variable; Duty Cycle = 50%

**Figure 12.  $I_{CCD}$  Test Circuit**



**Figure 13. AC Waveforms**

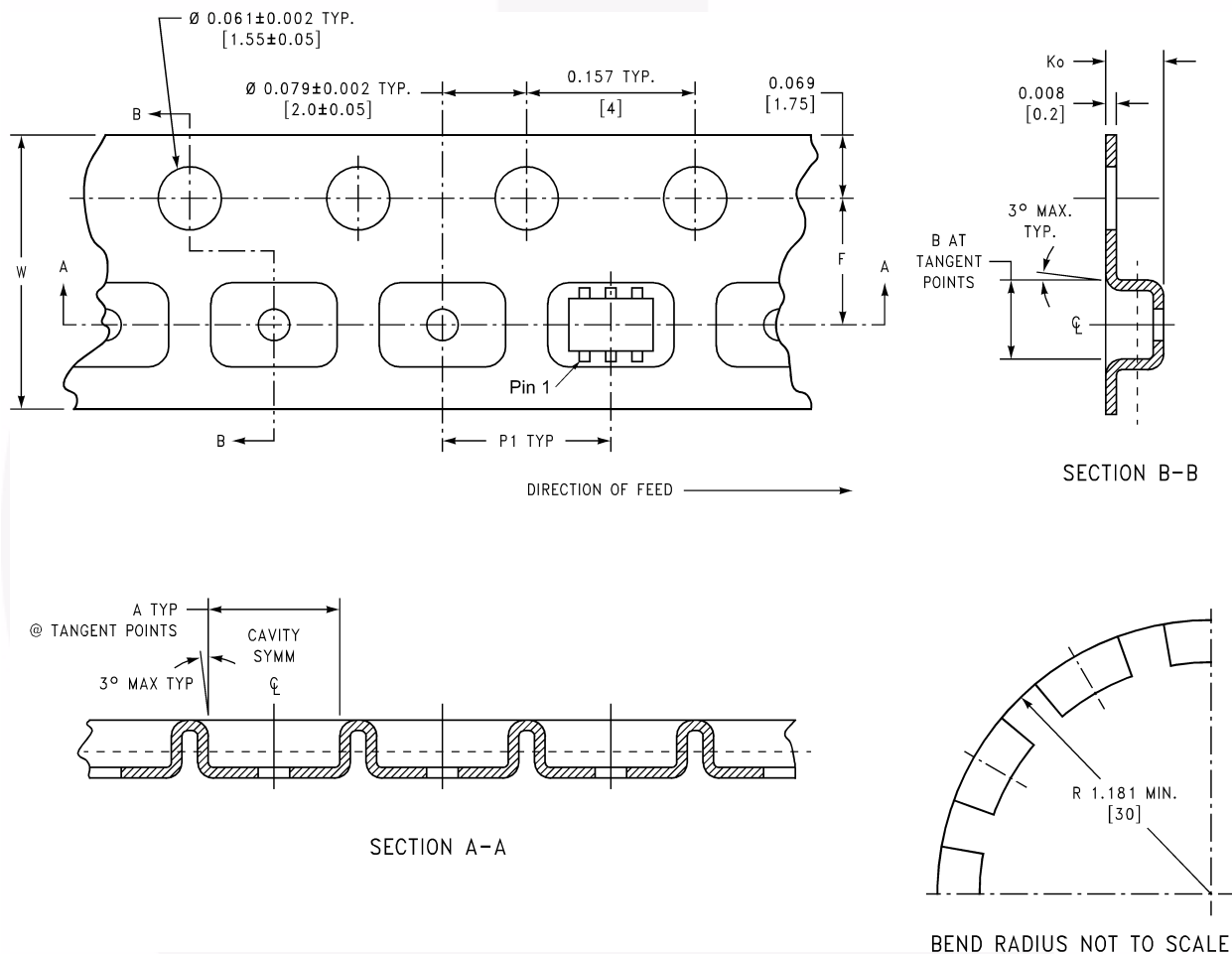


## Tape and Reel Specification

### Tape Format for SC70

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### Tape Dimensions inches (millimeters)

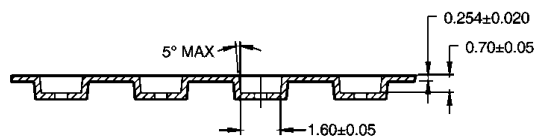
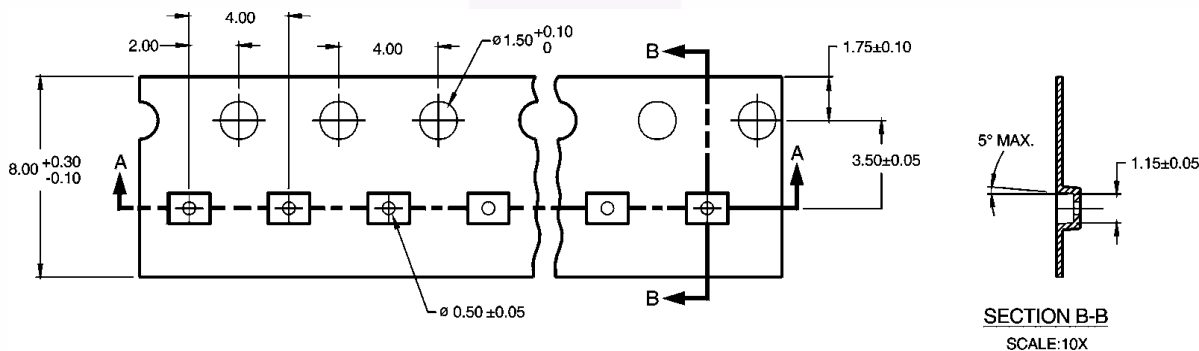


Package	Tape Size	Dim A	Dim B	Dim F	Dim K <sub>o</sub>	Dim P1	Dim W
SC70-6	8mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

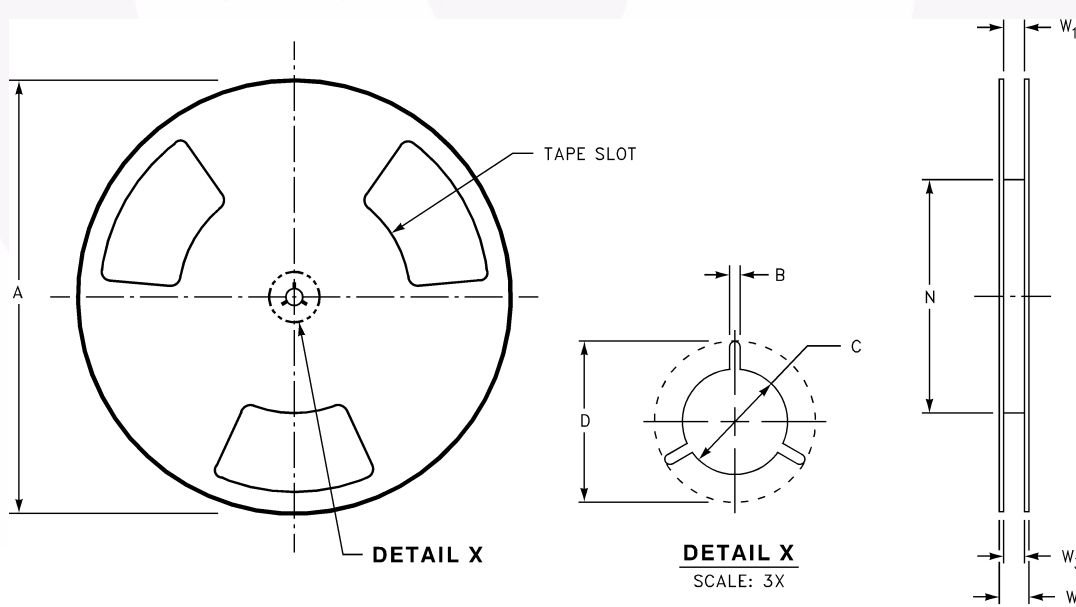
## Tape and Reel Specifications

### Tape Format for MicroPak

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

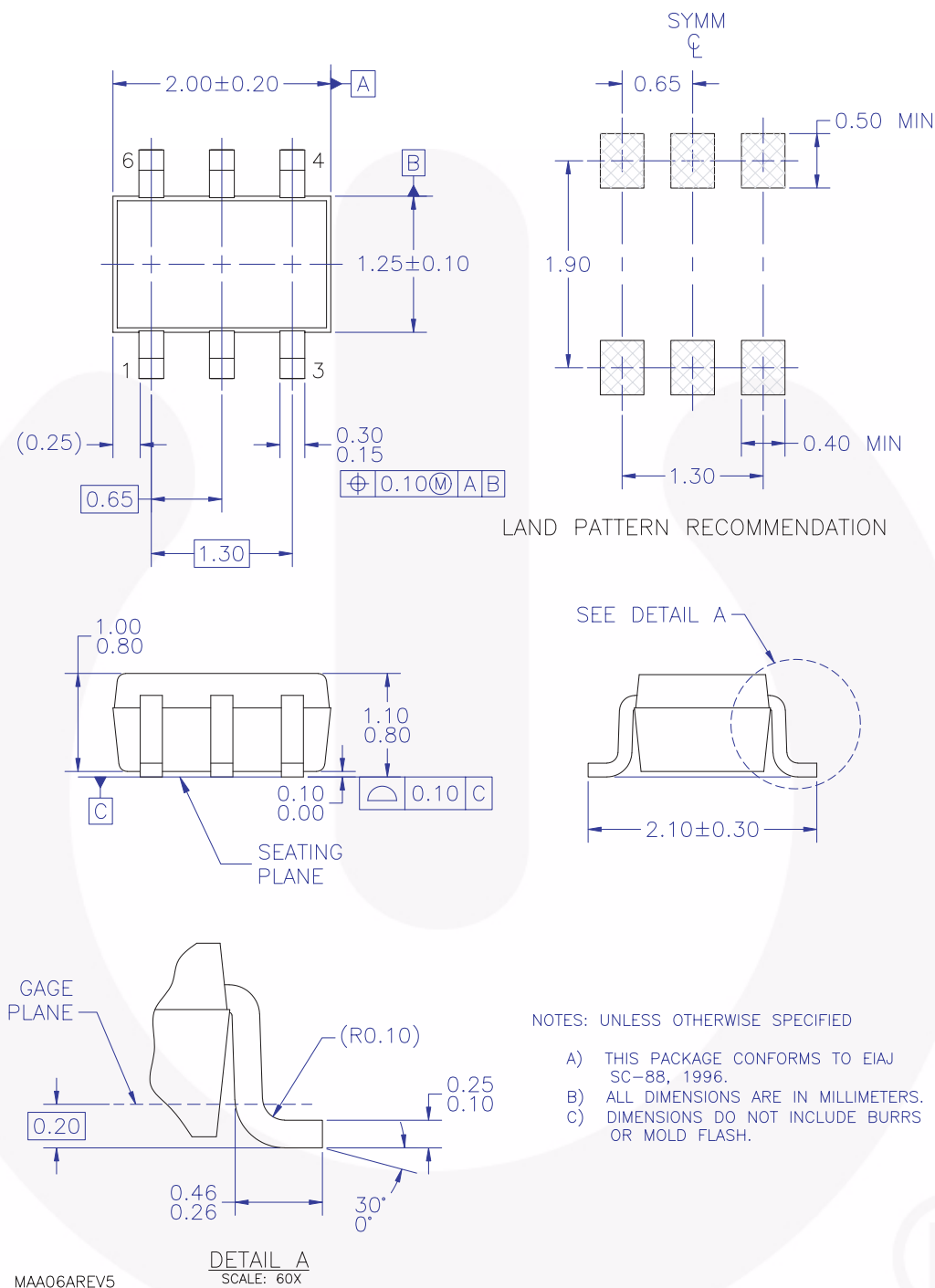


### Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

## Physical Dimensions

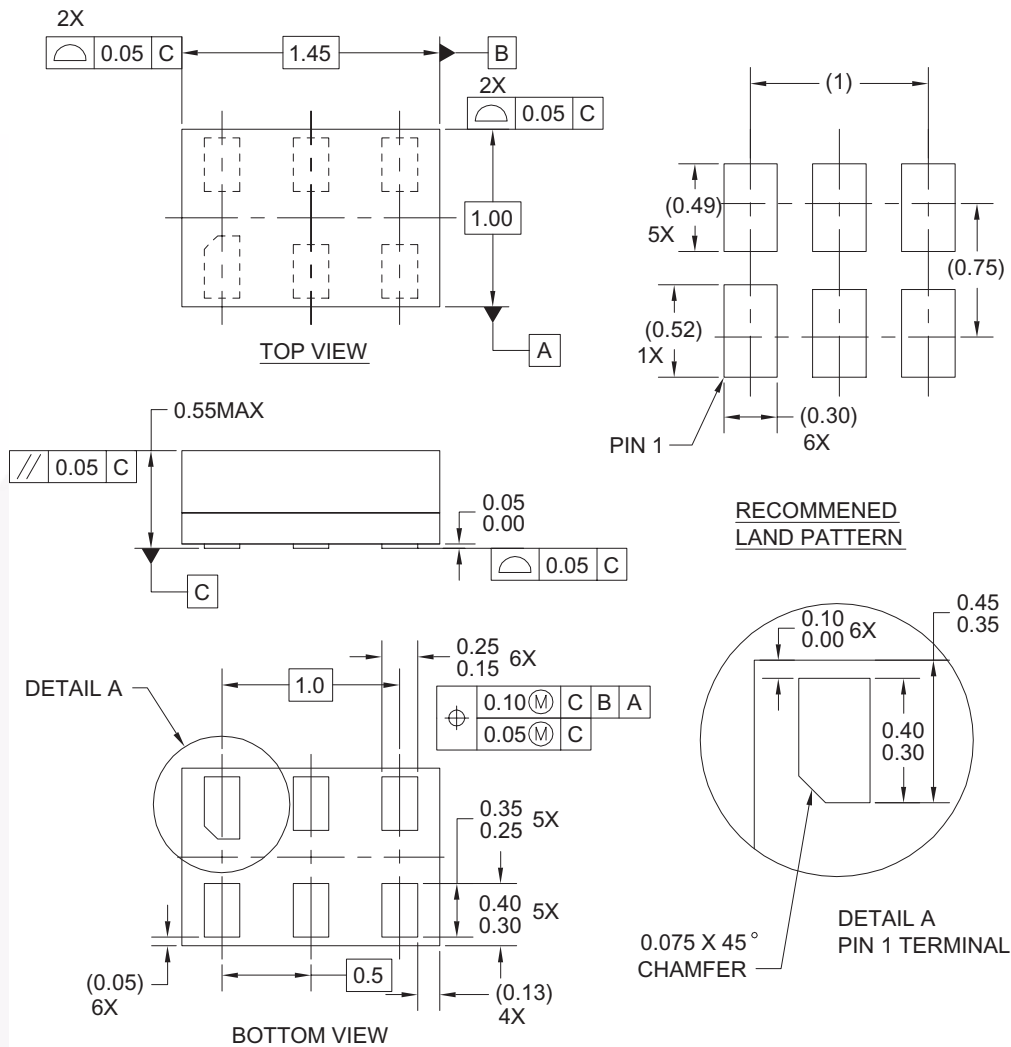


**Figure 14. 6-Lead SC70, EIAJ SC88, 1.25mm Wide**

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### Physical Dimensions (Continued)



**Notes:**

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06AREVC

**Figure 15. 6-Lead MicroPak, 1.0mm Wide**

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

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| EcoSPARK®   | i-Lo™                  | QFET®                      | TinyBuck™            |
| EZSWITCH™ *   | IntelliMAX™            | QS™                        | TinyLogic®           |
|  ™ | ISOPLANAR™             | QT Optoelectronics™        | TINYOPTO™            |
|  ™ | MegaBuck™              | Quiet Series™              | TinyPower™           |
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| FACT Quiet Series™  | MicroPak™              | SPM®                       | µSerDes™             |
| FACT®   | MillerDrive™           | STEALTH™                   | UHC®                 |
| FAST®   | Motion-SPM™            | SuperFET™                  | Ultra FRFET™         |
| FastvCore™ *  | OPTOLOGIC®             | SuperSOT™.3                | UniFET™              |
| FlashWriter® *  | OPTOPLANAR®            | SuperSOT™.6                | VCX™                 |
|   |                        | SuperSOT™.8                |                      |

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- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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